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(54) Semiconductor device having ventilative insulating films.

(57) A semiconductor device of multilevel wiring construction where a plurality of wiring layers are deposited so as to contain an interlevel insulating layers therebetween. The interlevel insulating layers of a semiconductor device according to the present invention have sandwich-like constructions, in which the lowermost film is the first silicon oxide film deposited by plasma vapor deposition method, the intermediate spin-coated film fabricated by means of spin-coating and curing method, and the uppermost film is the second silicon oxide film made by means of plasma vapor deposition method. The first silicon oxide film has high film density, while the second oxide film has low film density.

In the semiconductor device according to the present invention, the outgas generated at sputtering of the second wiring layers from the spin-coated film is released through the second silicon oxide film and does not concentrate in the through holes. Therefore, no corrosion of the wiring layers and no degradation of the step coverage occur; with the result that the disconnection of the second wiring layers in the through-holes are prevented.

According to the present invention, no disconnection of wire in the through-holes occurs even in the through-holes of diameter less than 1 micrometer, while in the prior art the disconnections of wires are indispensable for such small through-hole.

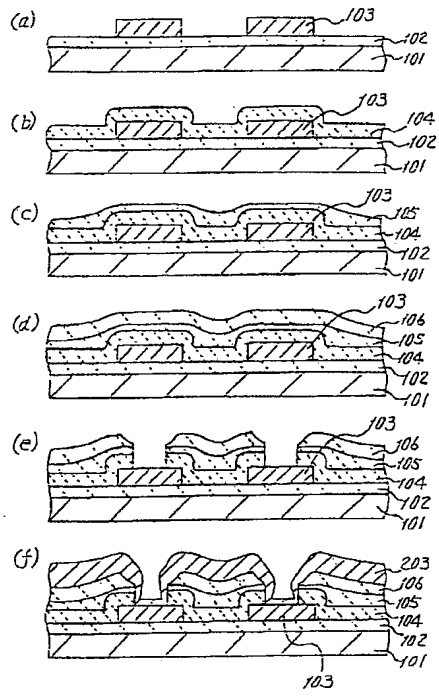

FIG. 1

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BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device, and more particularly to a semiconductor device comprising the multilevel interconnection composed of plural wiring layers with insulating layers inserted therebetween.

Description of the Prior Art

The use of multilevel interconnection in a semiconductor device, typically in LSI circuits, is important technique to realize a high density semiconductor device, because it gives the freedom to the arrangement and connection of the elements formed mainly upon the surface of the semiconductor substrate. The sizes of the elements are intended to be small to increase the integration density of a semiconductor device, and the wiring pattern to interconnect them upon chip needs a larger ratio of the chip area because the radio of the wiring pattern area to the total chip surface area becomes quite large. Since the reduction of the wiring pattern is limited due to the limitation of the current capacity and wiring resistance, the multilevel interconnection is highly desirable.

The advantages of the multilevel interconnection are the realization of high integration density and reduction of chip size. Moreover, there are other advantages, such as increase of the wiring freedom and easy design of wiring pattern. The setting of the wiring resistance and current capacity can be made with ample margin.

However, the semiconductor device employing multilevel interconnection has the disadvantages, such as low yield and low reliability, because the construction and fabrication process are complex and the surface of the device is not flat. Most of these disadvantages are due to the degradation of step coverage and the degradation of the depth of focus in exposure process at irregular and uneven portion of device surface and step-like portion of through-hole. Therefore, the planarization technology of insulating layers between the multilevel wiring layers and the device surface are indispensable for multilevel interconnection of semiconductor device.

The prior planarization technologies are the following:

(1) glass flow method

By reducing the viscosity of the insulating layer by means of the curing at a temperature above softening temperature of the insulating layer, the insulating layer is made to reflow due to self weight, so as to planarize the surface of the insulating layers.

(2) spin coating method

The organic solution containing photo-resist, polyimide resin or glass component is thickly spin-coated upon a surface of a semiconductor substrate and the spin-coated film is hardened by curing to obtain the flat surface.

(3) bias sputtering method

By utilizing the property that the sputter etching speed depends on the incident angle of high energy particle, such as argon, the un-even surface is planarized during the deposition of the insulating layer on the surface.

Among the above-mentioned planarization methods, the spin-coating method is desirable because the glass flow method needs the curing process at high temperature and damage the semiconductor device, and the bias sputtering method has a long throughput and generates high contamination.

In a semiconductor device of multilevel interconnection fabricated by means of spin-coating method, which is described in an article entitled "INTERLEVEL DIELECTRIC PLANARIZATION WITH SPIN-ON GLASS FILMS", by L. B. Vines and S. K. Gupta, Proc. IEEE 1986 V-MIC Conf., pp. 506-515 (1986), insulating layer is the sandwich-like construction composed of the first silicon dioxide film deposited by means of plasma vapor deposition method, an insulating film formed by spin-coating method, and the second silicon oxide film deposited by means of plasma vapor deposition method. This semiconductor device is fabricated according to the following processes.

Upon a semiconductor substrate on which the metal wiring is made, the first silicon oxide film is deposited by means of plasma vapor deposition method. An intermediate insulating film (called as spin coated film) is formed on the first silicon oxide film by spin coating the organic siloxane polymer followed by curing. Furthermore, the second silicon oxide film is formed on the spin coated film by means of plasma vapor deposition method. Thereafter, through-holes are made through the insulating layer composed of the first silicon oxide film, the spin coated film and the second silicon dioxide film. Then, the metal film is made for the second wiring layer and is patterned and the electric interconnection between two wiring layers is completed via through-holes. In this conventional semiconductor device, the first silicon oxide film and the second silicon oxide film are formed under the same condition and are relatively dense.

For the insulating layer of sandwich construction using spin coated film, a thick spin coated film is preferable by means of the surface flatness.

However, the fact that the film is thick may cause to increase the possibility of disconnections of the wires in the through-holes. The reason for this will be explained in the following.

In the fabrication process of the insulating layer of sandwich construction, the organic solvent in the spin coated film is exhausted by curing after the spin coating process and the film is hardened. In this process, a small quantity of organic solvent remains in the cured spin coated film. Moreover, the spin coated film adsorbs the water in the atmosphere even after it is dried and hardened by the curing. These residual organic solvent and water become gas when the metal film is sputtered as the second wiring layer, because the semiconductor substrate is heated in the vacuum. The outgas generated in this manner is flown out through sidewall of spin coated film exposed in through-holes. The spin coated film is corroded owing to the outgas, particularly to its water component. Also, since the through-holes are filled with outgas, the adhesion of metal atom flown from target to the sidewall of through-holes are prevented during formation process of wiring metal film by sputtering, with the result that the step coverage of wiring metal film in through-holes become degraded. If the concentration of outgas from spin coated film increases, the corrosion of metal film in the through-holes and the degradation of the step coverage are progressed. In other words, the disconnection of wire is more probable as the spin coated film is thick and the diameter of through-hole is small. In the conventional insulating layer of sandwich construction, it is difficult to realize a semiconductor device using the through-hole of its diameter being less than 1 micrometer.

The inventor has discovered that the disconnections in the through-holes increase if the density of the second silicon oxide film increases. Because the outgas generated from spin coated film during sputtering process can not penetrate through the second silicon oxide film, resulting in its concentration within the through-holes.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor device of the multilevel interconnection construction which is free from the disconnection of wires.

Another object of the present invention is to provide a semiconductor device comprising a planarized insulating layer which is free from the disconnection of wires in the through-hole due to the corrosion and degradation of step coverage.

The semiconductor device according to the present invention is characterized in that among insulating layer of sandwich construction the second silicon oxide film deposited by plasma vapor deposition method is formed as

In the semiconductor device according to the present invention, the dense silicon oxide film is deposited as the first insulating film by means of plasma vapor deposition method upon a semiconductor substrate on which the first wiring layer is formed. Upon the first silicon insulating film, the spin coated insulating film is formed by means of spin coating method. On this spin coated film, the lower density silicon oxide film is formed as the second silicon oxide film by means of plasma vapor deposition method on the spin coated insulating film. On an insulating layer composed of the first silicon oxide film, the spin coated film and the second silicon oxide film, the second wiring layer is deposited.

According to the present invention, the outgas generated from a spin coated film during a heating process, like the sputtering process, of the second wiring layer is exhausted through the second silicon oxide film. Therefore, the outgas does not concentrate in the through-holes. This means that the corrosion of wires and degradation of step coverage due to outgas do not occur, with the result that the disconnection of wire in the through-hole does not occur. In addition, since the dense silicon oxide film is used as the first silicon oxide film, the void does not occur even if metal, such as aluminum, is used for the first wiring layer.

It is desirable and effective that the contractions of the first and the second oxide films after the heating process which is under the condition of nitrogen atmosphere at 900 °C are less than and larger than 3%, respectively because in this percentage of the contractions the through-holes can be formed under the condition of the diameter which is less than 1 micrometer without disconnection of wires and an un-even surface.

BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other objects, features and advantages of this invention will become more apparent by reference to the following detailed description of the invention taken in conjunction with the accompanying drawings wherein:

Figs. 1(a) to (f) are cross-sectional views for illustrating the fabrication processes of the first preferred embodiment of the invention;

Fig. 2 is a diagram indicating the relation between the yield of good quality in the second aluminum wiring and the diameter of the through-hole in the multilevel wiring of the prior art and the present invention; and

Figs. 3(a) and (b) are diagrams indicating the infra red absorption spectra of the first and the second silicon oxide films deposited by employ-

ing tetraethoxyorthosilicate (TEOS) according to the second preferred embodiment of the invention, respectively.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figs. 1(a) to 1(f), a semiconductor device according to the first preferred embodiment of the present invention is made as follows. On a monocrystalline semiconductor substrate 101 containing semiconductor elements (not shown) formed therein, an insulating film 102 is formed. The film 102 is 500 nanometers in thickness. The film 102 is the resultant product of glass flow process of a BPSG film (boro-phosphosilicate glass), which is made by means of low pressure vapor deposition method using the process gas of diborane (B_2H_6) and phosphine (PH_3). Then, the aluminum film is deposited on the film 102 by sputtering method till its thickness being from 0.5 to 1.0 micrometer. After a photo lithography process, the aluminum wirings 103 are formed by etching by means of a parallel-plate-type dry etching equipment (Fig. 1(a)). The minimum width and minimum line spacing of the wiring 103 are 0.5 micrometers, respectively.

Next, the first silicon oxide film 104 which is about 400 nanometers in thickness is deposited by means of a parallel-plate-type plasma vapor deposition equipment (Fig. 1(b)). This film 104 is formed using the process gas of monosilane gas (SiH_4), dinitromonooxide gas (N_2O) and nitrogen gas (N_2) as dilution gas for monosilane gas which are flown at flow rate 70 sccm, 1300 sccm and 280 sccm, respectively. After the three gases are flown, total gas pressure is set to be 0.25 Torr, and the vapor deposition is performed under the condition of the discharge power density 0.5 w/cm^2 of its frequency 400 kHz at substrate temperature 300 $^\circ$C. Next, the first silicon oxide film 104 deposited is cured in nitrogen atmosphere at 900 $^\circ$C. The contraction percentage of the resultant film 104 is 0.8%, which indicates that the first silicon oxide film 104 is quite dense.

Then, a spin coated film 105 is made of organic siloxane polymer solution on the first silicon oxide film by the spin coating method. The solution is spin coated and heated. On this occasion, if the spin coating and heating are repeatedly performed several times, the solvent in the organic siloxane polymer solution can be almost released. In the present embodiment, the spin coating and heating are performed twice times. At first, the first spin coating of organic siloxane polymer solution is made and then the heating in the nitrogen atmosphere is performed again at 400 $^\circ$C. This application and curing are repeated under the sane condition to make an organic siloxane polymer layer which is the spin coated film 105. (Fig. 1(c)). The thickness of the organic siloxane polymer layer on the first insulating film 104 is 200 nanometers.

Next, the second silicon oxide film 106 is deposited by means of the plasma vapor deposition method with a parallel-plate-type vapor deposition equipment and is 400 nanometers in thickness (Fig. 1(d)). The deposition condition of the second silicon oxide film 106 is as follows.

The flow rate of monosilane gas (SiH_4): 70 SCCM

The flow rate of dinitromonooxide gas (N_2O): 1300 SCCM

The flow rate of nitrogen gas (N_2) as dilution gas for monosilane gas: 280 SCCM

total gas pressure: 0.35 Torr

discharge frequency: 400 kHz

discharge power density: 0.5 W/cm^2

the substrate temperature: 250 $^\circ$C

If the silicon dioxide film 106 deposited under this condition is heated in the nitrogen atmosphere at the temperature of 900 $^\circ$C to the test, the contraction rate of the film 106 is 3.5%, which indicates that the density of the film 106 is lower than the first silicon oxide film 104.

After the second silicon oxide film 106 is deposited, it is heated for 10 minutes in the nitrogen atmosphere at 400 $^\circ$C in order to fully release methane (CH_4), carbon dioxide (CO_2), water (H_2O) and methanol (CH_3OH) contained in the organic siloxane polymer film 105. On this occasion, the impurity gas in the spin coated film 105 is released through the second silicon oxide film 106, so that the spin coated film 105 and the second silicon oxide film 106 are not subjected to the delamination each other and constitute insulating layer of high quality with the first silicon oxide film 104.

Next, the through-holes (Fig. 1(e)) are made at desired position by means of a lithography and a dry etching method with a parallel-plate-type dry etching equipment. The minimum diameter of the through-hole is 0.5 micrometers.

Next, the second wiring layer 203 is selectively formed as follows. The sputtered aluminum film is formed on the second silicon oxide film 106 and is 0.5 to 1.0 micrometer thick. This film burys the through-holes. Then this film is formed by means of a lithography and dry etching with the parallel-plate-type dry etching equipment. The minimum width and minimum line spacing of the second wiring layer patterns are 0.5 micrometers, respectively.

Since the outgas generated by the sputtering process from the spin coated film 105 is not concentrated in the through-holes and is released through the second silicon oxide film 106, so that the aluminum wirings in the through holes are not

disconnected.

To check no existence of the corrosion and no deterioration of step coverage of the second wiring layer 203 in the through-holes after the fabrication process, the surface and cross-section view are observed with a optical microscope and a scanning electron microscope. As a result, no corrosion of the second wiring layer 203 occurs and good step coverage is obtained even when the diameter of the through hole is less than 1 micrometer.

Fig. 2 shows the relation between the diameter of the through-hole and yield of good quality for the multilevel wirings in each case of the prior art and the present invention. The electric conductivity between the first wiring layer 103 and the second wiring layer 203 is measured for the various diameters of the through-holes to examine the relation between the diameter of the through-hole and yield rate of good quality. Referring to Fig. 2, the yield of the wiring in case of the prior art considerably degrades if the diameter of the through-hole is less than 1.0 micrometer. Even in this condition, the yield of the present invention does not degrades and no disconnection of wire occur. Therefore, it is obvious that the interlevel insulating layer according to the present embodiment has the superior flat surface and no corrosion and no degradation of step coverage in the through-holes if their diameters are less than 1.0 micrometer. Also, since the first wiring layer 103 is covered with the dense first silicon oxide film 104, no void occur after the heating process.

In the second embodiment of the present invention, the first and the second silicon oxide films 104 and 106 can obtain more better flatness by employing the gas system containing tetraethoxyorthosilicate (TEOS).

The deposition condition of the first silicon oxide film is as follows.

The flow rate of helium (He) gas for bubbling TEOS (37 ° C): 500 SCCM

The flow rate of oxygen gas: 500 SCCM

The gas pressure of oxygen gas: 9 Torr

discharge frequency: 13.56 MHz

high frequency power density: 2 W/cm^2

substrate temperature: 355 ° C

The deposition condition of the second silicon oxide film 106 is almost the same as the first film 104 using TEOS except the condition of the high frequency power density which is 1.3 W/cm^2.

Referring to Fig. 3(a), the infra-red absorption spectrum of the silicon oxide film deposited under the above condition is almost identical to that of silicon oxide film deposited by thermal oxidization method. Also, the film contraction rate of this first silicon oxide film 104 after heating in the nitrogen atmosphere at 900 ° C is 1.28%. This value means that the dense film is deposited.

The deposition condition of the second silicon oxide film 106 is the same as the first film 104 except that the high frequency power density is changed to 1.3 W/cm^2. Referring to Fig. 3(b), the infra-red absorption spectrum of the second silicon oxide film 116 indicates that it contains Si-OH bond and H_2O more than the first silicon oxide film 104 does. This means that the lower density film is deposited. The film contraction rate of this silicon oxide film after heating in the nitrogen atmosphere at 900 ° C is 4.76%. The insulating film employing these first and second silicon oxide films have quite good flatness characteristics, with the result that two and/or more layer wirings can be realized without disconnection of wires for through-holes of diameter less than 1 micrometer.

Although the invention has been described with reference to specific embodiments, this description is not meant to be constructed in a limiting sense. Various modifications of the disclosed embodiment, as well as other embodiments of the invention, will become apparent to persons skilled in the art upon reference to the description of the invention. It is therefore contemplated that the appended claims will cover any modifications or embodiments as fall within the true scope of the invention.

Claims

1. A semiconductor device comprising first wiring layers, a first silicon oxide film selectively formed on said first wiring layers except through-hole regions, a spin-coated film formed on said first silicon oxide film, a second silicon oxide film having density of lower than the density of said first silicon oxide film and formed on said spin-coated film, and second wiring layers selectively formed on said second silicon oxide film.

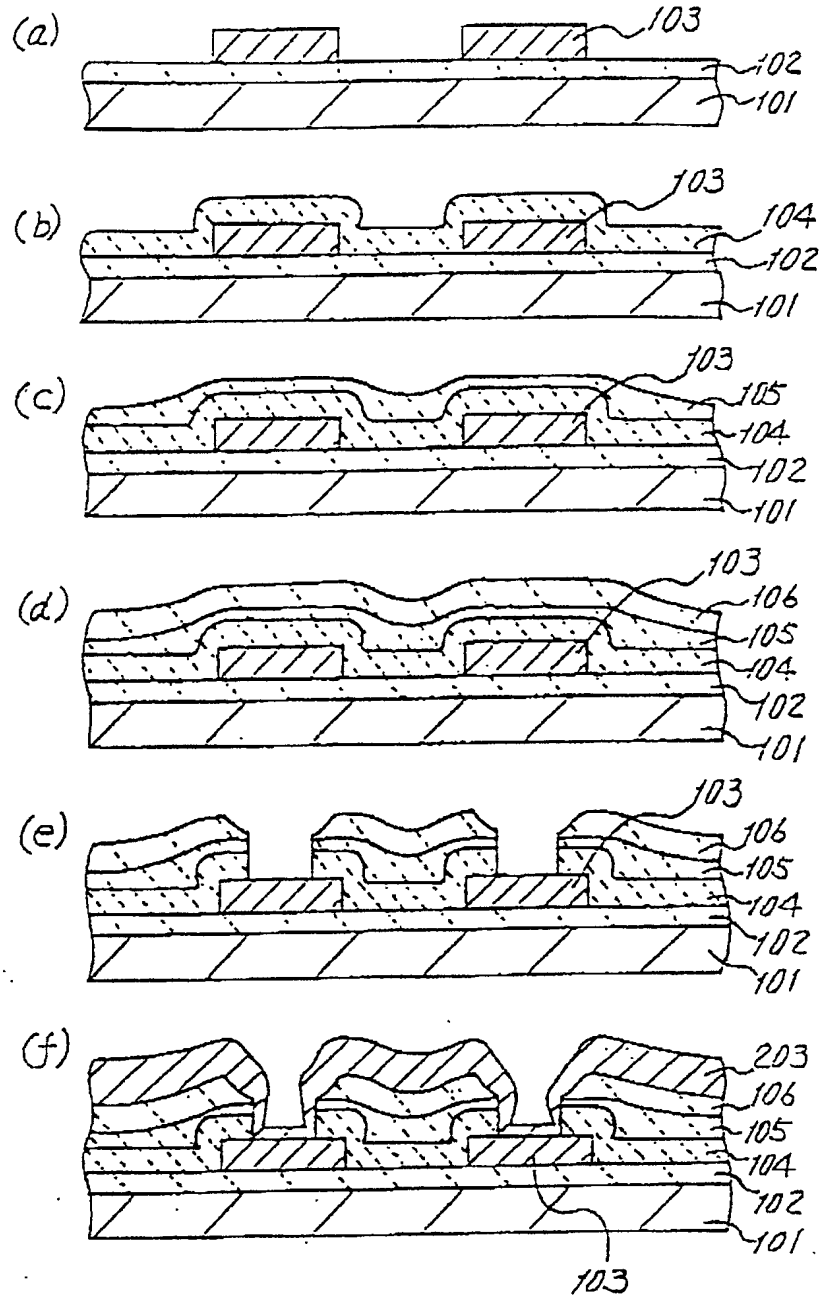
2. A semiconductor device as claimed in claim 1, wherein said first silicon oxide film has a contraction rate of 3% or less.

3. A semiconductor device as claimed in claim 1, wherein said second silicon oxide film has a contraction rate of 3% or more.

4. A semiconductor device as claimed in claim 1, said spin-coated film is made of organic siloxane polymer.

5. A semiconductor device comprising a semiconductor substrate being selectively covered with first insulating film, a first wiring layers formed on said first insulating film, a first silicon oxide film formed by means of a plasma vapor deposition method on the first wiring

layers except through-hole regions, a spin coated film formed by means of a spin coating method on said first silicon oxide film, a second silicon oxide film having a density lower than the density of said first silicon oxide film and formed by means of a plasma vapor deposition method on said spin-coated film and second wiring layers selectively formed on said second silicon oxide film and in said through-hole regions.


(a)
103
102
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(b)
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(c)
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(f)
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103

FIG. 1

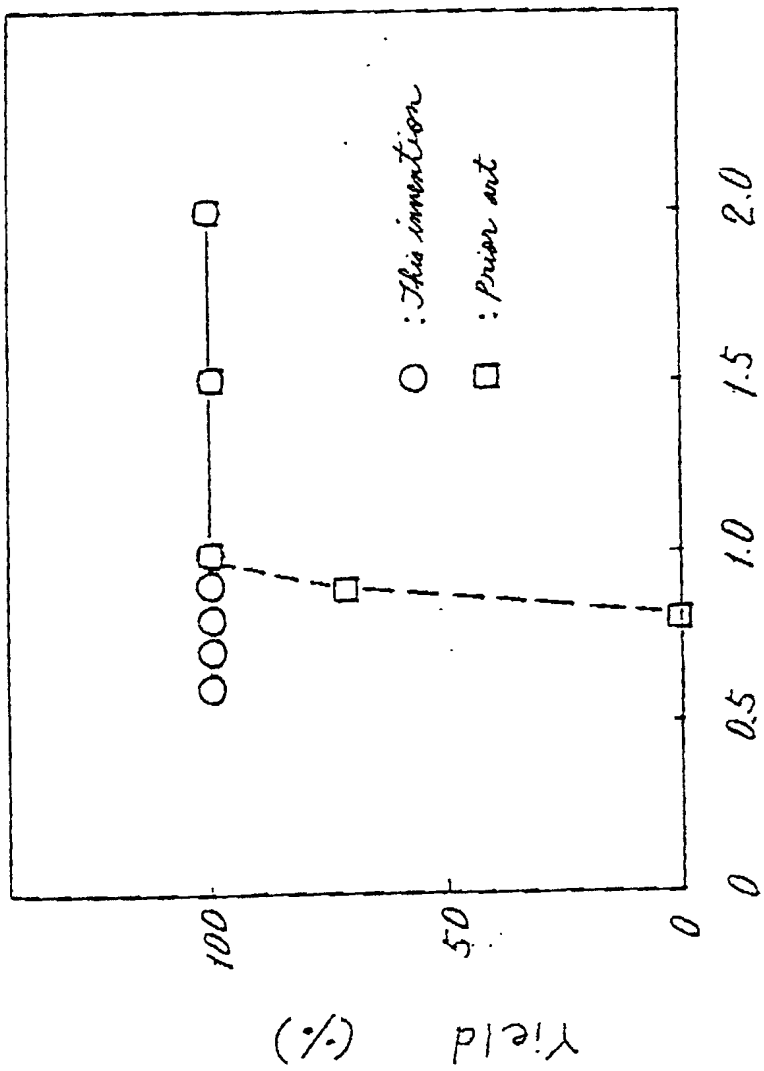
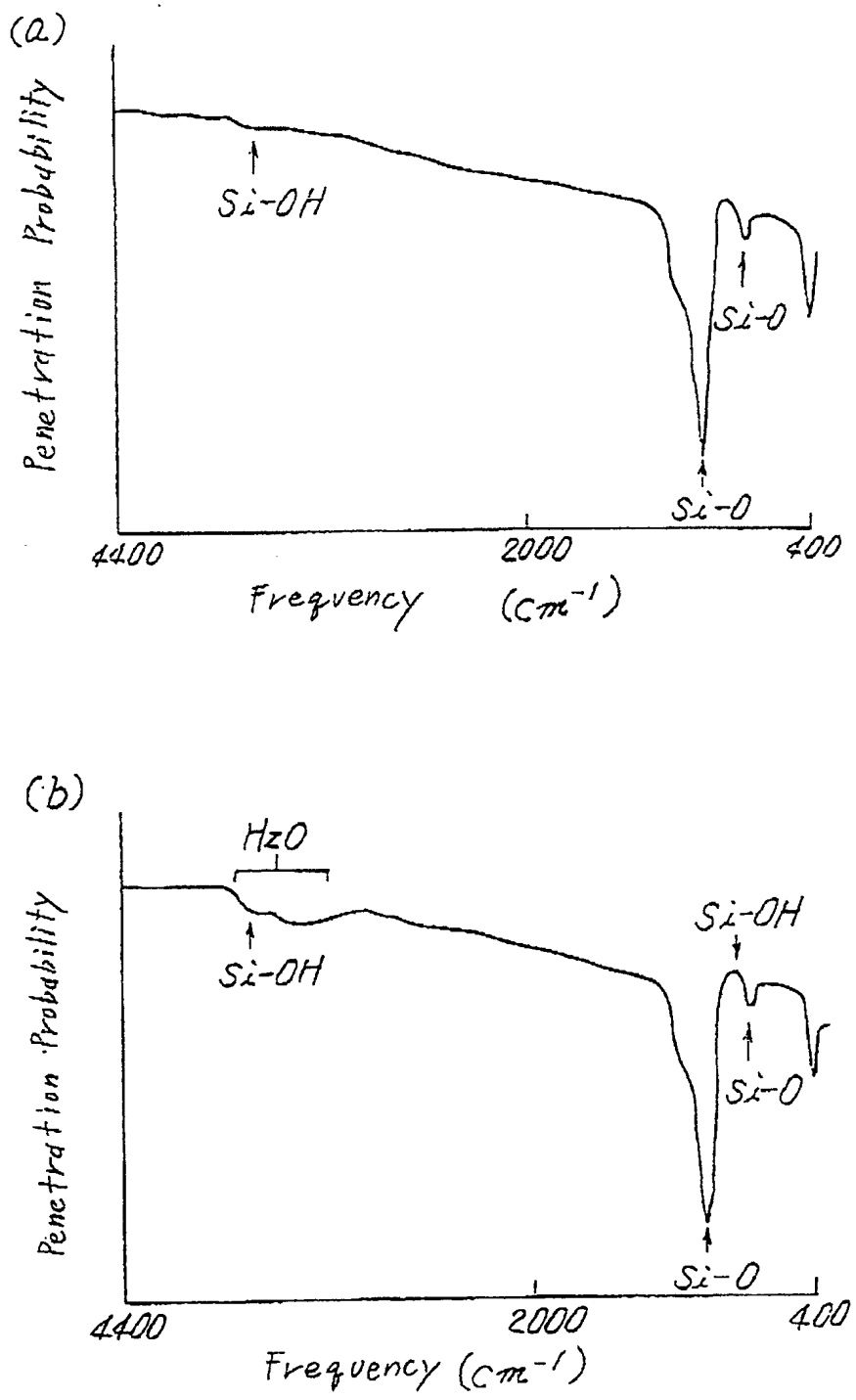

Yield (%)
100
50
0
0
0.5
1.0
1.5
2.0
The diameter of through-hole (μm)
○ : This invention
□ : Prior art

FIG. 2


(a)
Penetration Probability
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Si-O
Si-O
4400
2000
400
Frequency (cm⁻¹)
(b)
H₂O
Si-OH
Si-OH
Si-O
Si-O
Penetration Probability
4400
2000
400
Frequency (cm⁻¹)

FIG. 3